IN THE CLAIMS:

Please cancel claims 21–25.

Please amend the claims as set forth below:

1. (Original) A cache memory subsystem comprising:

a cache controller; and

a cache memory including a plurality of memory chips coupled to said cache controller for storing a plurality of cache lines, wherein separate subsets of said plurality of cache lines form separate classes of cache lines, and wherein address tags of cache lines of different classes are stored in different ones of said memory chips.

2. (Original) The cache memory subsystem as recited in claim 1, wherein said cache controller is configured to concurrently access a first address tag corresponding to a first cache line and a second address tag corresponding to a second cache line.

3. (Original) The cache memory subsystem as recited in claim 2, wherein said first cache line corresponds to a first snoop request and wherein said second cache line corresponds to a second snoop request.

4. (Original) The cache memory subsystem as recited in claim 1, wherein said first address tag is stored in a first of said plurality of memory chips and wherein said second address tag is stored within a second of said plurality of memory chips.

5. (Original) The cache memory subsystem as recited in claim 1, wherein each of said plurality of cache lines includes a tag field to store a corresponding address tag and a data field to store corresponding data.

6. (Original) The cache memory subsystem as recited in claim 5, wherein said tag field further stores state information indicative of a coherency state of said corresponding data.

7. (Original) The cache memory subsystem as recited in claim 6, wherein a portion of each of said plurality of said cache lines is stored in each of said plurality of memory chips.

8. (Original) The cache memory subsystem as recited in claim 7, wherein said cache controller is configured to receive a plurality of snoop requests, wherein each of said plurality of snoop requests includes an address having an index portion and a tag portion.

9. (Original) The cache memory subsystem as recited in claim 8, wherein said cache controller is configured to convey a first index corresponding to a first cache line to a first of said memory chips and to concurrently convey a second index corresponding to a second cache line to a second of said memory chips.

10. (Original) The cache memory subsystem as recited in claim 9, wherein said first cache line corresponds to a first snoop request received by said cache memory subsystem and wherein said second cache line corresponds to a second snoop request received by said cache memory subsystem.

11. (Original) A cache memory subsystem comprising:

a cache controller; and

a cache memory coupled to said cache controller for storing a plurality of cache lines, wherein said cache memory includes a plurality of memory sections, wherein each of said memory sections is separately addressable through separate address lines coupled to said cache controller, and wherein each memory section of said cache memory is configured to store a portion of each of said plurality of cache lines;

wherein said cache controller is configured to control accesses to said cache memory such that a first set of address tags corresponding to a first subset of said plurality of cache lines is stored in a first of said plurality of memory sections and such that a second set of address tags corresponding to a second subset of said plurality of cache lines is stored in a second of said plurality of memory sections.

12. (Original) The cache memory subsystem as recited in claim 11, wherein said cache controller is configured to concurrently access a first address tag corresponding to a first cache line and a second address tag corresponding to a second cache line.

13. (Original) The cache memory subsystem as recited in claim 12, wherein said first cache line corresponds to a first snoop request and wherein said second cache line corresponds to a second snoop request.

14. (Original) The cache memory subsystem as recited in claim 11, wherein said first address tag is stored in a first of said plurality of memory sections and wherein said second address tag is stored within a second of said plurality of memory sections.

15. (Original) The cache memory subsystem as recited in claim 11, wherein each of said plurality of cache lines includes a tag field to store a corresponding address tag and a data field to store corresponding data.

16. (Original) The cache memory subsystem as recited in claim 15, wherein said tag field further stores state information indicative of a coherency state of said corresponding data.

17. (Original) The cache memory subsystem as recited in claim 16, wherein a portion of each of said plurality of said cache lines is stored in each of said plurality of memory sections.

18. (Original) The cache memory subsystem as recited in claim 17, wherein said cache controller is configured to receive a plurality of snoop requests, wherein each of said plurality of snoop requests includes an address having an index portion and a tag portion.

19. (Original) The cache memory subsystem as recited in claim 18, wherein said cache controller is configured to convey a first index corresponding to a first cache line to address a first of said memory sections and to concurrently convey a second index corresponding to a second cache line to address a second of said memory sections.

20. (Original) The cache memory subsystem as recited in claim 19, wherein said first cache line corresponds to a first snoop request received by said cache memory subsystem and wherein

said second cache line corresponds to a second snoop request received by said cache memory subsystem.

21-25. Cancelled.